A Multi-Layered Air-Gap Transmission Line Design for CMOS-Compatible Millimeter-Wave ICs

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***Abstract*—A compact and chip-area efficient transmission line design is proposed for monolithic millimeter-wave integrated circuits. Performance improvement is achieved by the use of multi-layered air-gaps compatible to CMOS fabrication. Based on a 65-nm CMOS process, the on-chip transmission line occupies less than 17 µm in width and 8 µm in height while active devices and circuits can still be fabricated with interconnect routing right beneath the shielded structure of the transmission line. The semi-enclosed structure allows the tuning of the characteristic impedance. 3D electromagnetic simulations give results of 1.8 dB/mm insertion loss and a reflection coefficient of -28 dB at 60 GHz, for a 50-ohm matched design. The multi-layered air-gap design allows the current density more uniformly distributed in the signal-carrying conductor compared with a counterpart design without air-gaps.**

Keywords—CMOS transmission line, air-gap, monolithic microwave integrated circuits, millimeter wave, dual damascene

I. Introduction

Transmission lines are indispensable for building circuits and systems for microwave and millimeter wave applications, including the unlicensed 60-GHz frequency band. In fact, in the development of monolithic microwave and millimeter wave integrated circuits (MMICs) using modern silicon CMOS technology [1]-[2], on-chip transmission lines are used in such as mixers [3], power amplifiers [4]-[5] and RF/microwave switches [6]. Based on the standard CMOS fabrication, various physical structures such as deep n-well [7], floating shields [8], interleaved metal patterns [9], slow-wave coplanar waveguides [10]-[11], have been investigated for on-chip transmission lines to minimise the insertion loss and crosstalk. However, all these on-chip transmission line designs occupy much chip area.

A very compact semi-enclosed stripline design with a rectangular coaxial structure was proposed in [12]-[13] for implementation in multi-metallisation CMOS processes. With the microelectronics community's keen interest in integrating air-gaps between copper lines for advanced interconnects [14]-[15], the area-efficient transmission line design [12] can be further improved with air-gapped interconnects. While some air-gap transmission lines were investigated to give high performance [16]-[17], these designs are either difficult in realisation or using up much space in silicon CMOS technology. In this work, a CMOS-compatible air-gap transmission line design is investigated using structures with feasible fabrication [18]-[20] in CMOS technology yet without a significant increase in the cost.

II. Multi-Layered Air-Gap Transmission Line Design

The proposed compact air-gap transmission line design is illustrated in Fig. 1, with the air-gaps shown in white colour for the top four metallisation levels (metal 5 to metal 8) in the cross-sectional structure. It is based on a commercially available 65-nm CMOS process in which there are eight levels of copper metallisation above the active devices fabricated in the silicon substrate [12]. In principle, the design can be implemented in other integrated circuit (IC) processes that have multi-metallisation levels [13]. As shown in the cross-sectional diagram (Fig. 1), the top five layers of metals (M4 to M8) are used to construct the transmission line structure, leaving the remaining three metal layers at the bottom for interconnect routing of active devices and circuits. Metal 7 is used for the signal-carrying core because its thickness is relatively large (2.75 µm) to alleviate the disadvantages of the skin effect. The opening gap (with its size s_{gap}) in the metal-8 ground conductor and the width of the signal-carrying core conductor (w_{core}) can both be used to tune the characteristic impedance Z_0 for impedance matching purposes [12]. The adjustment of w_{core} and s_{gap} can vary the distributed inductance, capacitance and resistance of the transmission line.

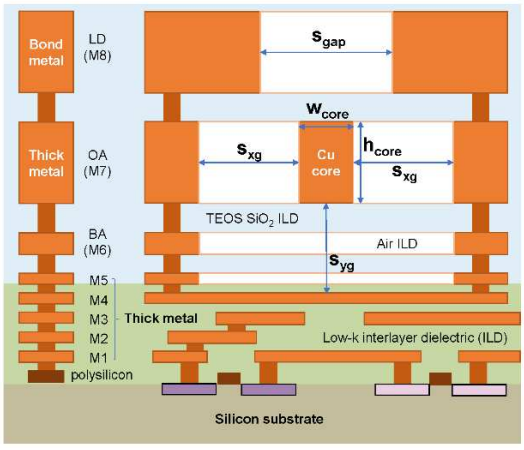

Fig. 1. Cross-sectional diagram of the proposed multi-layered air-gap transmission line design in a 65-nm CMOS process with eight metal layers

Due to fabrication constraints related to CMOS compatibility, the air-gaps in the design are only within the space of otherwise the metal layers (M5 to M8 in Fig. 1). There is no air-gap between different metal layers. As a result, the air-gap has its thickness the same as that of the corresponding metal layer, for example 2.75 µm for metal 7, but a thinner air-gap corresponding to metal 6 and even a thinner one to metal 5. With the relative permittivity ε_r of air very close to 1.0, the air-gaps obviously can help reduce the distributed capacitance (C') in the transmission line. The distributed capacitance reduction would have the most significant effect for the air-gaps between the signal-carrying core conductor (M7) and the bottom ground conductor (M4).

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This is because the total thickness of the metal layers (M5 and M6) and the inter-layer dielectrics is fixed by the CMOS fabrication and cannot be adjusted in the IC layout. In the 65-nm CMOS process for the transmission line design, the total thickness is 1.5 µm. As for the sideway capacitance between the signal-carrying core conductor and the ground conductors on the left and right sides, it can be reduced simply by making the spacing (s_{xg}) much larger than 1.5 µm in the IC layout. Intuitively, the distributed capacitance reduction would allow a larger w_{core} (instead of 500 nm in [12]) of the signal-carrying core while maintaining a desirable characteristic impedance Z_0 = 50 Ω. The wider signal-carrying core conductor is then expected to give a smaller distributed resistance (R') in the transmission line and hence improvement in the insertion loss. Overall, the total width (the side-to-side dimension in the cross-section) of the transmission line design is about 17 µm.

The air-gap structure can be implemented by a via-first dual damascene process between SiO_2 inter-layer dielectrics (ILD) [18]. In such a process, a high-modulus tetracyclododecene (TD)-based sacrificial polymer is used as a placeholder for air-gap formation. Three additional steps are used beyond the traditional dual damascene process, including spin-coating, etching, and thermal decomposition of the sacrificial polymer. Compared with the metallisation-first process, the dielectric-first process (via-first dual damascene process) is capable for the metal formation with a wide range of aspect ratios. Moreover, it is easier to fill voids with metal than to fill voids with dielectric in the back end of line (BEOL). The air-gap formation for the transmission line design is similar with fabrication alike [19]-[20]. Although there would be some increase in the fabrication cost, it is quite minimal while the distributed capacitance reduction is significant.

The available process parameters are copper metal layers sheet resistance R_s and TEOS (tetraethylorthosilicate) SiO_2 inter-layer capacitance C_{ILD} [12]. They are used to estimate the thickness of each metal layer and ILD with the estimated values shown in Table I.

TABLE I. TESTED PARAMETER DATA AND ESTIMATED THICKNESS VALUES IN AN EIGHT-LEVEL COPPER METALLISATION CMOS PROCESS

Tested Parameter	Tested Structure Data	65nm Process Parameter	Estimated Value
M8 Sheet Resistance R_{sM8}	7.3 mΩ/sq	M8 (copper) Thickness t_{M8}	2.23 µm
M8-M7 Capacitance C_{ox87}	75 αF/µm^2	ILD (SiO_2) Thickness t_{ox87}	450 nm
M7 Sheet Resistance R_{sM7}	6.27 mΩ/sq	M7 (copper) Thickness t_{M7}	2.75 µm
M7-M6 Capacitance C_{ox76}	61 αF/µm^2	ILD (SiO_2) Thickness t_{ox76}	550 nm
M6 Sheet Resistance R_{sM6}	40 mΩ/sq	M6 (copper) Thickness t_{M6}	430 nm
M6-M5 Capacitance C_{ox65}	161 αF/µm^2	ILD (SiO_2) Thickness t_{ox65}	210 nm
M5 Sheet Resistance R_{sM5}	87 mΩ/sq	M5 (copper) Thickness t_{M5}	200 nm
M5-M4 Capacitance C_{ox54}	251 αF/µm^2	ILD (low-k) Thickness t_{ox54}	110 nm
M4 Sheet Resistance R_{sM4}	87 mΩ/sq	M4 (copper) Thickness t_{M4}	200 nm

With the conductivity of copper $\sigma = 5.8 \times 10^7$ S/m, the metal thickness t_M is then calculated by:

$$t_M = \frac{1}{\sigma \times R_s} \quad (1)$$

The relative permittivity of the ILD is set accordingly with standard values, i.e. ε_r = 3.8 for TEOS SiO_2 ILD, ε_r = 2.8 for low-*k* ILD, and ε_r = 1.0 for the air-gap layers. The permittivity in vacuum is $\varepsilon_0 = 8.85 \times 10^{-12}$ F/m. The ILD thickness t_{ILD} can be calculated using the following:

$$t_{ILD} = \frac{\varepsilon_r \times \varepsilon_0 \times S}{C_{ILD}} \quad (2)$$

where S = 10^{-12} m^2 is the 1µm-by-1µm area of the interlayer metal-plate capacitance. The estimated thicknesses are approximated to a close integer value under tolerance and fabrication process consideration.

III. ELECTROMAGNETIC-FIELD SIMULATION

To evaluate the multi-layered air-gap transmission line design (Fig. 1) for silicon-based MMICs, electromagnetic (EM) simulation using finite element method (FEM) was performed with the Ansys HFSS software. For the purpose of matching Z_0 = 50 Ω, the cross-section structural dimensions are set correspondingly: w_{core} = 2.9 µm and h_{core} = 2.75 µm for the signal-carrying core conductor, w_{ground} = 500 nm for M5 to M7 ground conductors, s_{gap} = 7.9 µm, s_{xg} = 6.3 µm, s_{yg} = 1.5 µm for the structure of transmission line. The simulated length of transmission line is set as l = 200 µm. Considering the skin effect, a conductor carrying an alternating current, especially at the frequencies of the millimeter-wave range, tends to transmit the power only close to the near-surface. The unit skin depth δ_s is defined as the depth where the current density falls to 1/*e* of its value near the surface, which means almost 63% current density is reduced at a depth of δ_s. The skin depth δ_s is about 270 nm at 60 GHz for copper, which can be theoretically calculated by:

$$\delta_s = \sqrt{\frac{1}{\pi \times \sigma \times \mu \times f}} \quad (3)$$

where $\sigma = 5.8 \times 10^7$ S/m for copper conductivity, μ_r = 0.99 H/m for the relative permeability of copper, $\mu_0 = 4\pi \times 10^{-7}$ H/m for the vacuum permeability, f = 60 GHz being the target frequency. As shown in Fig. 2, the skin depth δ_{s60GHz} = 270 nm can be verified by the current density distribution visually.

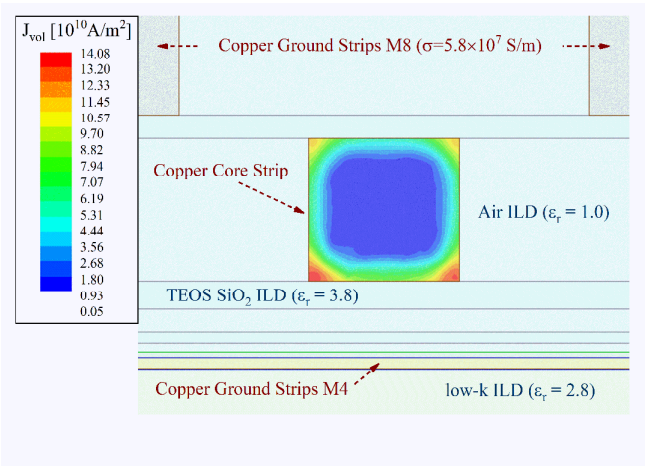

Fig. 2. Current density distribution in the multi-layered air-gap transmission line design (a cross-sectional view)

The relative current density distributions along the horizontal and vertical central axes are shown in Fig. 3. The current density along the vertical axis varies more sharply than that of the horizontal axis. This is because the capacitance between the signal and ground conductors is larger along the vertical axis at the bottom part of the transmission line's cross-sectional structure (Fig. 1). Along the vertical axis, the current density at the bottom of the signal-carrying core conductor is also considerably larger than that at the top for the same reason. Owing to the structural symmetry, along the horizontal axis, the current density distributions in the left and right parts of the core conductor have no significant difference.

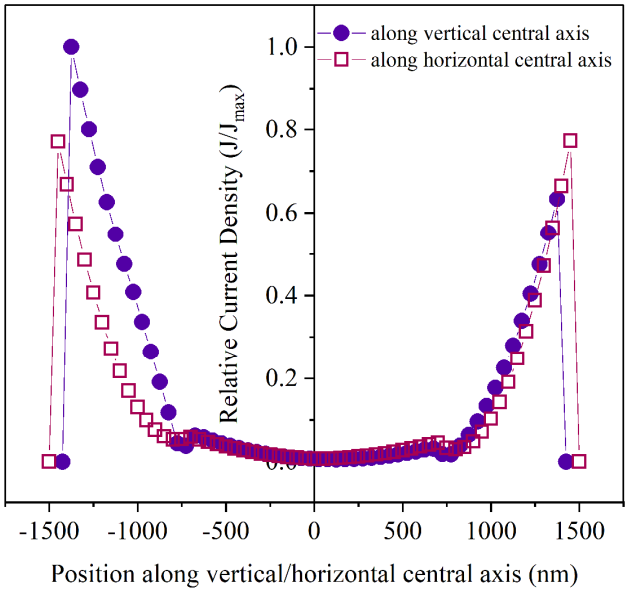

Fig. 3. Current density distributions along the vertical and horizontal central axes of the core conductor in the multi-layered air-gap transmission line design

As the thickness of the metal 7 layer is fixed and as large as t_{M7} = 2.75 µm, the aspect ratio of the signal-carrying core conductor is commonly less than 1 (i.e. $w_{core}/h_{core} < 1$). While keeping the same opening gap in metal 8 for tunable Z_0 of the transmission line, Z_0 = 50 Ω can be obtained by enlarging the width of the core conductor (w_{core}). With the increase of the aspect ratio (w_{core}/h_{core}), the highest current density position moves from the bottom surface of the core conductor to the two bottom corners. Such adjustment gives a transmission line with the current density more uniformly distributed. In the 65-nm CMOS process, Z_0 being matched to 50 Ω can be achieved easily when the aspect ratio w_{core}/h_{core} = 2.9/2.75. When the relative current density decreases to 37% along the horizontal or vertical axes (Fig. 3), the changed position of $d \approx \delta_{s60GHz}$ also confirms the theoretical skin depth value calculated by Equation (3).

IV. Simulation Results and Analysis

The tuning of the air-gap transmission line's Z_0 by the different opening gap sizes in the upper ground plane is demonstrated in the EM simulation results (Fig. 4). When the upper opening gap size increases, the real part of Z_0 also increases because the capacitance between the core and upper ground conductors decreases. In this situation, the current density concentrates at the bottom part of the core conductor. The imaginary part of Z_0 is about -*j*4 Ω. When the frequency is set at 60 GHz and the real part of Z_0 is 50 Ω, the corresponding opening gap size is less than 8 µm. As shown in Fig. 5, the reflection coefficient $|S_{11}|$ is as small as -28 dB, and a low insertion loss is achieved with $|S_{21}|$ = -0.36 dB for a 200-µm air-gap transmission line, i.e. $|S_{21}|$ = -1.8 dB/mm. Such low insertion loss is valid at both low and high frequencies. The bandwidth is about 80 GHz for $|S_{21}|$ in a reasonable range (no worse than -2 dB/mm). In this multi-layered air-gap transmission line, the effective relative permittivity ε_{reff} is 1.95, and the wavelength λ is 3.6 mm at 60 GHz. The reduced ε_{reff} may allow useful properties of the transmission line for multi-10Gbs on-chip RF serial links [21].

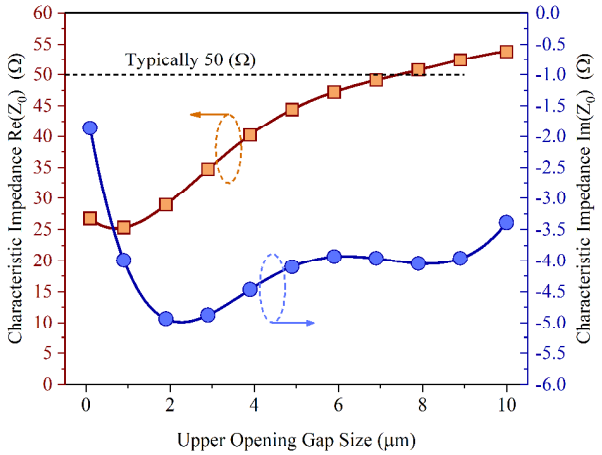

Fig. 4. Tuning of the characteristic impedance Z_0 in the multi-layered air-gap transmission line by varying the size of the opening gap which is between the metal-8 ground conductors on the left and right sides

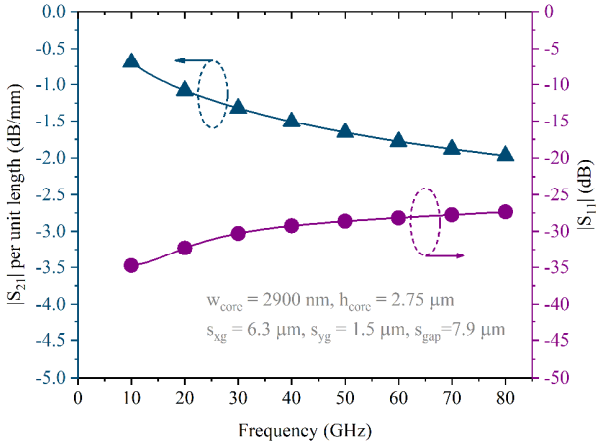

Fig. 5. Two-port S-parameter results from 3D full-wave EM simulation for the optimised 50-Ω multi-layered air-gap transmission line

In the EM simulations using *HFSS*, the finite element computation is only determined by the nodes and elements of the mesh, i.e. the mesh structure and density. Once the computational results have no significant changes even by further mesh refinement, the mesh mapping would be acceptable and the results would be reasonably accurate. In the EM simulation of this work, the mesh was mainly under the element-length-based refinement. When the maximum length of the element of the signal-carrying core conductor is refined from the default 40 µm to 1 µm, the simulated $|S_{21}|$ value is improved from -1.8 dB/mm to -1.4 dB/mm, and the $|S_{11}|$ is optimised further from -28 dB to -43 dB at 60 GHz.

With the S-parameter data obtained from the EM simulations, the distributed elements of the multi-layered air-gap transmission line can be derived using the telegrapher's equation. The corresponding propagation constant γ and the characteristic impedance Z_0 can also be determined at the target frequency of 60 GHz. The values of the distributed elements are listed in Table II. With the optimised dimensions, the propagation constant is: γ = 179 (Np/m) + *j*1743 (rad/m), and the characteristic impedance is: Z_0 = 49 - *j*4.4 (Ω). It can be seen that the multi-layered air-gap transmission line design gives considerably lower distributed capacitance and resistance compared with the counterpart design without the air-gap (i.e. using normal ILD and hence a smaller w_{core} = 500 nm in [12]).

TABLE II. DISTRIBUTED ELEMENT AND OTHER PARAMETERS OF THE MULTI-LAYERED AIR-GAP TRANSMISSION LINE AT 60 GHZ WITH COMPARISONS OF THE COUNTERPART DESIGN [12] USING NORMAL ILD

Distributed Element	Air-Gap	Normal ILD
Resistance $R' = \mathrm{Re}\{\gamma Z_0\}$	16.4 kΩ/m	26.8 kΩ/m
Inductance $L' = \mathrm{Im}\{\gamma Z_0\}/\omega$	1.41 μH/m	2.24 μH/m
Conductance $G' = \mathrm{Re}\{\gamma/Z_0\}$	0.46 S/m	0.32 S/m
Capacitance $C' = \mathrm{Im}\{\gamma/Z_0\}/\omega$	0.59 nF/m	0.84 nF/m
Propagation Constant γ (/m)	179 + *j*1743	270 + *j*2624
Characteristic Impedance Z_0 (Ω)	49.0 + *j*4.4	51.8 + *j*5.0

V. CONCLUSION

A compact 50-Ω multi-layered air-gap transmission line design has been presented in detail. It has been verified by EM simulations for a design based on the process parameters of a 65-nm multi-metallisation CMOS process and on the fabrication by the via-first dual damascene process. The EM simulation results show the more uniformly distributed current density in the signal-carrying core conductor, leading to reduced distributed resistance and smaller insertion loss. The good results are attributed to the air-gap design in reducing the distributed capacitance, hence allowing the advantage of a close-to-unity aspect ratio (w_{core}/h_{core}) in the signal-carrying core conductor. Compared with typical on-chip transmission lines, the proposed design occupies significantly less chip area. This area-efficient transmission line design will be helpful for the development of silicon-based MMICs.

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REFERENCES

[1] B. Heydari *et al.*,"Millimeter-Wave Devices and Circuit Blocks up to 104 GHz in 90 nm CMOS," *IEEE Journal of Solid-State Circuits*, vol. 42, no. 12, pp. 2893- 2903, Dec. 2007.

[2] B. Razavi, "Design of Millimeter-Wave CMOS Radios: A Tutorial," *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 56, no. 1, pp. 4-16, Jan. 2009.

[3] B. M. Motlagh *et al.*, "Fully Integrated 60-GHz Single-Ended Resistive Mixer in 90-nm CMOS Technology," *IEEE Microwave and Wireless Components Letters*, vol. 16, no. 1, pp. 25-27, Jan. 2006.

[4] P. Chen *et al*., "A 22–31 GHz Distributed Amplifier Based on High-Pass Transmission Lines Using 0.18 μm CMOS Technology," *IEEE Microwave and Wireless Components Letters*, vol. 21, no. 3, pp. 160-162, Mar. 2011.

[5] M. Bassi *et al*., "A 40–67 GHz Power Amplifier With 13 dBm Psat and 16% PAE in 28 nm CMOS LP," *IEEE Journal of Solid-State Circuits*, vol. 50, no. 7, pp. 1618-1628, July 2015.

[6] R.-B. Lai *et al*., "A 60–110 GHz Transmission-Line Integrated SPDT Switch in 90 nm CMOS Technology," *IEEE Microwave and Wireless Components Letters*, vol. 20, no. 2, pp. 85-87, Feb. 2010.

[7] K. Nishikawa *et al*., "Characteristics of Transmission Lines Fabricated by CMOS Process With Deep n-Well Implantation," *IEEE Transactions on Microwave Theory and Techniques*, vol. 54, no. 2, pp. 589-598, Feb. 2006.

[8] T.S.D. Cheung and J.R. Long, "Shielded Passive Devices for Silicon-Based Monolithic Microwave and Millimeter-Wave Integrated Circuits," *IEEE Journal of Solid-State Circuits*, vol. 41, no. 5, pp. 1183 - 1200, May 2006.

[9] H.-M. Hsu *et al*., "Millimeter-Wave Transmission Line in 90-nm CMOS Technology," *IEEE Journal on Emerging and Selected Topics in Circuits and Systems*, vol. 2, no. 2, pp. 194-199, June 2012.

[10] D. Kaddour *et al*., "High-Q Slow-Wave Coplanar Transmission Lines on 0.35 μm CMOS Process," *IEEE Microwave and Wireless Components Letters*, vol. 19, no. 9, pp. 542-544, Sept. 2009.

[11] Jinglin Shi *et al*., "Millimeter-Wave Passives in 45-nm Digital CMOS," *IEEE Electron Device Letters*, vol. 31, no. 10, pp. 1080-1082, Oct. 2010.

[12] S. Lam and M. Chan, "Compact transmission line design in a multi-metallization nano-CMOS process for millimeter-wave integrated circuits," *40th International Conference on Infrared, Millimeter, and Terahertz Waves (IRMMW-THZ 2015)*, Hong Kong, Aug. 2015.

[13] S. Lam and M. Chan, "A 50-ohm semi-enclosed stripline design in a 90-nm CMOS process for silicon-based monolithic microwave integrated circuits," *2015 Asia-Pacific Microwave Conference (APMC)*, Nanjing, Dec. 2015.

[14] L.G. Gosset *et al*. "General review of issues and perspectives for advanced copper interconnections using air gap as ultra-low K material," *Proceedings of the IEEE 2003 International Interconnect Technology Conference*, Burlingame, CA, USA, 4 June 2003.

[15] J. Park, Improving CMOS Speed and Switching Power with Air-Gap Structures. PhD dissertation, UC Berkeley (2011).

[16] J. C. P. Chuang and S. M. El-Ghazaly, "Integration of air-gap transmission lines on doped silicon substrates using glass microbump bonding techniques," *IEEE Transactions on Microwave Theory and Techniques*, vol. 46, no. 11, pp. 1850-1855, Nov 1998.

[17] I. Jeong et al., "High-Performance Air-Gap Transmission Lines and Inductors for Millimeter-Wave Applications," *IEEE Transactions on Microwave Theory and Techniques*, vol. 50, no. 12, pp. 2850 - 2855, Dec. 2002.

[18] S. Park, S. A. B. Allen, and PA Kohl, "Air-gaps for high-performance on-chip interconnect part II: modeling, fabrication, and characterization," *Journal of Electronic Materials*, vol. 37, no. 10, pp. 1534-1546, Oct. 2008.

[19] C. Prawoto *et al*. "Interconnect Technology With h-BN-Capped Air-Gaps," *IEEE Electron Device Letters*, vol. 40, no. 11, pp. 1876-1879, Nov. 2019.

[20] C. Prawoto *et al*. "High Frequency Monolithic Inductor with Air-Gaps," *2020 4th IEEE Electron Devices Technology & Manufacturing Conference* (*EDTM*), Penang, Malaysia, 6-21 Apr. 2020.

[21] M. Tmimi *et al*., "10Gbps Length adaptive on-chip RF serial link for Network on Chips and Multi-processor chips applications," *2019 International Conference on IC Design and Technology* (*ICICDT*), Suzhou, China, 17-19 June 2019.